4. b)

To verify the accuracy of the buck converter design, the expected component values were compared with the values calculated from the simulation results. The analysis focused on three key parameters: the output inductor Lf, the output capacitor Cf, and the maximum load resistance Rmax, using measured values of the output voltage Vo, the inductor current ripple ΔiL, the output voltage ripple ΔVo, and the minimum output current IoAVmin.

The measured output voltage was 47.62 V, slightly below the nominal 48.00 V, with a difference of only 0.38 V. This deviation of less than 1% is within specification and is likely caused by resistive losses in the system, such as source resistance, MOSFET on-resistance, and diode forward voltage. These losses are expected in practical scenarios and confirm that the converter maintains stable operation.

The minimum output power measured was 98.59 W, compared to the design value of 100 W. Using the measured voltage, the output current was approximately 2.07 A, almost identical to the expected 2.08 A. This confirms the current-based calculations and supports the validity of the converter's behaviour under minimum load.

The calculated maximum load resistance, based on the output voltage and current, was 23.00 Ω, closely matching the expected value of 23.04 Ω. This consistency shows that the converter is correctly supplying the designed power to the intended load.

The inductor value Lf, computed from the inductor current ripple and switching parameters, was 6.09e-4 H, while the design specified 6.00e-4 H. This small difference of less than 2% is acceptable and likely due to numerical rounding and small variations in measured ripple. It confirms that the inductor sizing ensures continuous conduction mode under minimum load conditions.

The only significant discrepancy was found in the capacitor value Cf. The expected design value was 5.42e-5 F, while the calculated value from the simulation was only 1.13e-6 F. This difference is primarily due to the measured output voltage ripple being much larger than expected (0.9658 V vs. a target of ~0.48 V). Since the calculated capacitance is inversely proportional to the voltage ripple, the higher observed ripple results in a much lower estimate of Cf. This may be due to simplified or idealized assumptions in the original design, or the effects of parasitic and snubber components present in the simulation, which can influence ripple characteristics.

In conclusion, the values of Lf, Rmax, and IoAVmin were confirmed by the simulation and align well with theoretical predictions. The output voltage also remained within acceptable limits. The difference in Cf highlights the sensitivity of ripple-based sizing to dynamic effects and reinforces the importance of including realistic behaviour and losses in both simulation and design stages.

4. c)

This laboratory focused on the modelling, simulation, and analysis of a DC-DC Buck Converter intended for use in a 48 V DC microgrid. The converter was designed to regulate output voltage while supplying resistive loads with powers ranging from 100 W to 1500 W. The work involved both theoretical design and practical simulation using MATLAB/Simulink and the Simscape Electrical toolbox.

Through steady-state simulations, we observed that the output voltage remained relatively stable around the design target of 48 V, while the output current and power adjusted according to the load. As expected, lower load resistance led to higher current and power, confirming the converter’s ability to regulate voltage under varying load conditions. We also analysed how inductor current ripple and voltage ripple evolved, particularly under minimum and maximum load, which deepened our understanding of the converter’s dynamic response and the role of component sizing.

In a dedicated task, we confirmed the validity of the designed values for the output inductor Lf​, output capacitor Cf ​, and maximum load resistance Rmax​, using measurements from simulation. The values of Lf and Rmax​ were closely aligned with the theoretical design, demonstrating consistency between analysis and simulation. The capacitor Cf​, however, showed a notable deviation due to larger-than-expected output voltage ripple, highlighting the influence of non-ideal effects such as parasitic resistances and snubber dynamics in practical simulations.

An important part of the lab involved testing the system’s dynamic response by introducing a load step through a switching breaker. The output voltage dropped significantly and stabilised below the nominal value, not because of control limitations (the system was open-loop), but due to increased power losses under high current conditions. This revealed how internal resistances and fixed duty cycles limit voltage regulation in open-loop operation, reinforcing the importance of feedback control in practical systems.

Overall, the lab provided valuable insights into both the theoretical operation and real-world behaviour of Buck converters. It strengthened our understanding of converter dynamics, ripple control, the impact of internal losses, and the importance of accurate component sizing. The work also developed our skills in simulation and analysis, preparing us to apply these tools in more complex power electronics systems.

4.d)

During the simulation of the buck converter for a 48 V DC microgrid, we evaluated its performance across multiple scenarios. The analysis covered steady-state voltage behaviour, ripple performance, the output power range using resistive loads, operation under minimum load conditions, and the system’s dynamic response to abrupt load changes via a breaker event.

**Output Voltage Variation and Ripple:**

In nominal steady-state operation, the output voltage remained very close to 48 V, with ripple well within 1% of the nominal voltage. This confirms the effectiveness of the designed LC output filter, where the chosen inductor Lf ​ and capacitor Cf ​ values sufficiently smooth the PWM waveform generated by the switching operation. The ripple behaviour stayed within specification for both minimum and nominal load conditions.

**Breaker Event and Voltage Stabilization:**

At time t=0.02s, the simulation introduced a significant step change in the load using a breaker to connect a resistor Req=Rmax/14 in parallel with Rmax. This sharply reduced the total load resistance, greatly increasing the current draw from the converter. As expected in an open-loop configuration, the output voltage experienced an abrupt dip, dropping to values below 30 V immediately after the breaker activation.

However, after a brief transient, the voltage did not return to its original value but instead stabilized at a lower level. This behaviour is not due to any voltage control (since the system is open-loop), but due to resistive voltage drops within the power path. Higher current implies increased power dissipation in the source internal resistance ri ​, the MOSFET's on-resistance Ron ​, and the parasitic resistance of the inductor. These losses grow quadratically with current (P = R\*I^2), causing a significant drop in the effective output voltage.

**Output Power Range with Resistive Loads:**

The converter was tested with resistive loads ranging from 100 W to 1500 W, corresponding to resistances of ~23 Ω to ~1.5 Ω. For high-resistance loads (light load), the converter demonstrated excellent voltage regulation and minimal ripple. As the load resistance decreased and current increased, the system began to show more noticeable ripple and voltage deviation.

**Minimum Resistive Load Operation:**

The system remained stable at the minimum design load of 100 W. The voltage remained within the required tolerance and the system operated in continuous conduction mode (CCM). This validates the design assumptions for Lf​ and Cf​, ensuring stable operation across the expected power range.

**Efficiency Behaviour:**

The converter achieved high efficiency (≈ 97–98%) under nominal load conditions. However, when current increased (especially during the breaker event), efficiency dropped due to higher conduction losses. This is expected in systems with non-negligible resistances under high current stress. Since the duty cycle is fixed, there is no compensating action to maintain voltage, causing both output voltage and efficiency to drop slightly.

4. e)

The buck converter designed and simulated in this study demonstrated good performance under steady-state conditions. With a nominal duty cycle and well-chosen LC filter values, the converter was able to maintain a stable output voltage of approximately 48 V and a ripple within the 1% design specification. Efficiency under nominal load conditions (1500 W) was notably high, typically around 97–98%, indicating that the chosen component values and open-loop setup are well-suited for ideal or slowly varying loads.

However, when a significant load step was introduced through the activation of a breaker at t=0.02s—adding an extra resistor in parallel to the main load—the system's limitations became evident. The output voltage dropped sharply and, although it recovered partially, it stabilized at a lower level than the original 48 V. This behaviour results not from any closed-loop regulation (which was absent) but rather from internal resistive elements within the circuit, such as the source resistance ri​, the MOSFET’s on-resistance Ron​, and any parasitic elements modelled in the power path. As current increases due to the lower total resistance, these internal losses (P=R\*I^2) grow significantly, reducing the available voltage at the output.

The inability of the system to respond to dynamic changes in load is a clear indication of the limitations of open-loop control. Because the duty cycle is fixed, it cannot adapt to sudden drops in load resistance or compensate for the additional losses caused by higher current flow. Consequently, both the output voltage and efficiency degrade during such events, and the system operates below its optimal point.

To improve the performance of the converter in realistic scenarios, we believe it would be wise to implement closed-loop control. A proportional-integral-derivative (PID) controller could dynamically adjust the duty cycle in response to changes in load, helping maintain the output voltage close to its target regardless of disturbances. Additionally, improving the model by including realistic internal losses, such as the MOSFET’s non-ideal characteristics, would provide more accurate simulation results and better inform hardware design.

In conclusion, while the converter performed well under constant conditions, its open-loop nature restricts its ability to handle dynamic loading. In a following phase, we believe that introducing feedback and refining the simulation model could be essential next steps to make this converter viable for real-world applications in DC microgrids, where varying loads and sudden transitions are common.